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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/709,869 | 06/02/2004 | Cheng Kangguo | FIS920040065US1 | 3868 |

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INTERNATIONAL BUSINESS MACHINES CORPORATION
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| EXAMINER | |
|---|---|
| NHU, DAVID | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/709,869 | KANGGUO ET AL. | |
| | Examiner | Art Unit | |
| | David Nhu | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAIL ACTIONS

### *Claims Objection*

*1. Claim 1, "the sidewall" should be –the trench sidewall--*

Claim 17, "**the** trench sidewall**, the** single-crystal semiconductor material" lack a clear antecedent basis.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 are rejected under 35 U.S.C. 102 (b) as being anticipated by Kudelka et al (6,426,254 B2).

**Regarding claims 1,** Kudelka, (see figures 2-8, col. 4, lines 6-67, col. 5, lines 1-67, col. 6, lines 1-46 ), teaches a method of making a buried plate region 112 in a semiconductor substrate 102, comprising: forming a trench 110 in a semiconductor substrate 102, the trench having a trench sidewall, the trench sidewall including an upper portion, and a lower portion 125 disposed below the upper portion 116 ( see figure 8); forming a liner 119 along at least the lower portion of the trench sidewall; thereafter forming a dopant source layer 107 over the liner, the dopant source layer not being disposed along the upper portion of the trench sidewall; and annealing the semiconductor substrate to drive a dopant from the dopant source

layer into the semiconductor substrate adjacent to the upper portion of the trench sidewall (see col. 4, lines 35-52).

Regarding claim 2, Kudelka, (see figure 6), a cap layer 110 is formed in the trench to prevent the dopant from being driven into the semiconductor substrate adjacent to the upper portion.

Regarding claims 3-11, Kudelka, (see figures 2-8), also teaches the liner having a thickness, wherein the liner is formed by thermal oxidation/nitridation; the cap layer consists oxide/nitride and undoped oxide; the annealing/heating at a temperature.

Regarding claim 13, Kudelka, (see figures 2-8), teaches removing the cap layer, the dopant source layer and the liner fropm the trench sidewall after the annealing, thereafter forming a collar 116 along the upper portion of the trench sidewall, andd then widening the lower portion of the trench sidewall.

Regarding claim 14, Kudelka teaches wherein the dopant source layer is formed by depositing arsenic doped glass (ASG) at a temperature (see figures 2, 5).

Regarding claim 15, Kudelka teaches forming a node dielectric along the lower portion of the trench sidewall after removing the liner and the dopant source layer; and depositing at least one of a conductive and a semiconducting material onto the node dielectric as a second plate opposing the buried plate (see figure 6).

Regarding claim 16, Kudelka teaches the liner and the dopant source layer are formed in the lower portion of the trench sidewall by forming the liner, forming the dopant source layer over the liner, depositing a cover material over the dopant source layer, recessing the cover material to a predetermined level, and removing the liner and the dopant source layer from the upper portion of the trench sidewall ( see figure 5).

**Regarding claim 17**, Kudelka, (see figures 2-8, col. 4, lines 6-67, col. 5, lines 1-67, col. 6, lines 1-46 ), teaches a method of making a trench 110 in a semiconductor substrate 102, and a buried plate 112 in the semiconductor substrate adjacent to a lower portion 125 of the trench sidewall, comprising: forming a pad stack 101 on a semiconductor substrate 102 and patterning the pad stack to form an opening 110; patterning a trench 110 through the opening by vertically etching the substrate selective to a material of the pad stack; forming a liner 119 on the semiconductor substrate along a sidewall of the trench; forming a dopant source layer 107 over the liner on a lower portion of the trench sidewall (see figure 6); forming a cap layer 110 covering at least an upper portion of the trench sidewall above the lower portion; and annealing to drive a dopant from the dopant source layer into the single crystal semiconductor material of the substrate adjacent to the lower portion to form a buried plate ( see figures 5, 6, col. 4, lines 35-52).

Regarding claim 17, Kudelka teaches the dopant source layer includes arsenic doped glass, the liner is formed by at least one of thermal oxidation/nitridation, and the cap layer consists of undoped oxide (see figure 2).

**Regarding claim 19**, Kudelka, (see figures 2-8, col. 4, lines 6-67, col. 5, lines 1-67, col. 6, lines 1-46 ), teaches a method of making a trench capacitor 110 in a semiconductor substrate 102, comprising: forming a pad stack 101 on a semiconductor substrate 102 and patterning the pad stack to form an opening; patterning a trench 110 through the opening by vertically etching the substrate selective to a material of the pad stack; forming a liner 119 on the semiconductor substrate along a sidewall of the trench; forming a dopant source layer 107 over the liner on a lower portion of the trench sidewall (see figure 6); removing the dopant

source layer from the liner along an upper portion of the trench sidewall, while allowing the dopant source layer to remain along a lower portion of the trench sidewall disposed below the upper portion;

forming a cap layer 110 covering at least an upper portion of the trench sidewall; and annealing to drive a dopant from the dopant source layer into the semiconductor material of the substrate adjacent to the lower portion to form a buried plate ( see figures 5, 6, col. 4, lines 35-52); removing the cap layer, the dopant source layer and the liner from at least the lower potion of the trench sidewall ( see figure 3); forming a node dielectric 107 along the lower portion of the trench sidewall; and forming a node electrode 125 on a side of the node dielectric opposite the buried plate 112 (see figure 6).

Regarding claim 20, Kudelka teaches the liner is formed by at least one of thermal oxidation/nitridation, the dopant source layer includes arsenic doped glass (ASG), and the cap layer consists of an undoped oxide; widering the lower portion prior to forming the node dielectric and prior to forming the electrode (see figures 6, 7, 8).

**Conclusion**

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kudelka'273, Mandelman'332, Michaelis'893, Schrems'704, Kleinhenz'484 are cited as of interest.

5 A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see 710.02 (b)).

6. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (571)272-1787.

*The fax phone number for the organization where this application or proceeding is assigned is (703)972-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956. Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).*

*David Nhu* DN

April 18, 2005